## REMARKS

Claims 1-12 are pending in this application. Claim 1 is independent.

## Claim Rejection - 35 USC 112

Claims 1 through 12 have been rejected under 35 U.S.C. 112, second paragraph. Applicant has amended claims 1 and 12 in order to correct the indefinite language. Accordingly, Applicant respectfully requests that the rejection be withdrawn.

## Claim Rejection - 35 USC 102

Claim 1 has been rejected under 35 U.S.C. 102(b) as being anticipated by Shimura et al. (U.S. Patent 5,864,169, "Shimura"). Applicant respectfully traverses this rejection.

Claim 1 is directed to a method for fabricating a heterojunction bipolar transistor, which among other steps, includes a step of forming a via hole which extends through the emitter layer, the base layer and the collector layer and ends at the specified depth within the substrate (e.g., see Fig. 2C). The collector layer, base layer and emitter layer had been formed and patterned such the upper layer has an area that is smaller than the area of the lower layer (e.g., see Fig. 2A).

> Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. Dismissed, 468 U.S. 1228 (1984); W.L. Gore and Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. Denied, 469 U.S. 851 (1984).

The Office Action states that this claim limitation is taught in Shimura at figures 4a and 4b.

At column 18, lines 28 to 37, Shimura discloses that the holes 25a are formed in regions of the substrate at both sides of each HBT element. Thus, it can be seen that the holes 25a do not extend through the emitter, base, and collector layers. Thus, Applicant submits that at least for this reason, Shimura fails to teach or suggest each and every claimed element. Applicant respectfully requests that the rejection be withdrawn.

**CONCLUSION**

All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the present application is in condition for allowance and such allowance is respectfully solicited. Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert W. Downs (Reg. No. 48,222), to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1. 17; particularly, extension of time fees.

Respectfully submitted,

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ABSTRACT OF DISCLOSURE

A heterojunction bipolar transistor is fabricated by laminating an emitter layer, a base layer, and a collector layer on a top surface of a semiconductor substrate, forming a via hole through the emitter layer, the base layer, the collector layer and the substrate at a specific depth, and providing a heat sink layer made of a metal on a rear surface of the substrate. A surface electrode of the emitter layer and the heat sink layer are connected to each other by a metal wiring line running through within the via hole, thereby improving the heat radiation and reducing the emitter inductance.